Design Example Report

Title	***8.4 W CV/CC LED Driver Using LNK606PG***
Specification	85 – 265 VAC Input; 12 V, 0.7 A Output
Application	Low Cost LED Driver
Author	Applications Engineering Department
Document Number	DER-215
Date	May 1, 2009
Revision	1.0

Summary and Features

- Revolutionary control concept provides very low cost, low part count solution
  - Primary side control eliminates secondary side control and optocoupler
  - Provides ±5% CV and ±10% CC accuracy
  - Over-temperature protection – tight tolerance (±5%) with hysteretic recovery for safe PCB temperature under all conditions
  - Auto-restart output short circuit and open-loop protection
  - Extended pin creepage distance for reliable operation in humid environments – >3.2 mm minimum at package
- EcoSmart® – Easily meets all current international energy efficiency standards – China (CECP) / CEC / ENERGRY STAR EPS v2 / EU CoC / EISA 2007
  - No-load consumption <100 mW at 265 VAC

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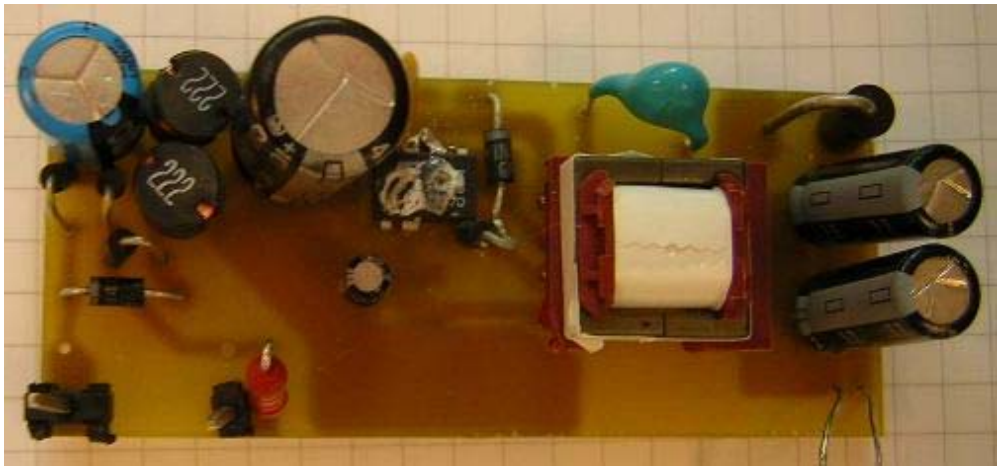
Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This report describes an 8.4 W CV/CC, universal input, power supply for LED Applications. A LNK606PG from the LinkSwitch-II family was used.



Assembled PCB

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2 Power Supply Specification

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	85		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power (230 VAC)				250	mW	
Output						
Output Voltage 1	V_{OUT1}	11.4	12.00	12.6	V	±5%
Output Ripple Voltage 1	$V_{RIPPLE1}$		150		mV	20 MHz bandwidth
Output Current 1	I_{OUT1}	630	700	770	mA	±10%
Total Output Power						
Continuous Output Power	P_{OUT}		8.4		W	
Efficiency						
Full Load	η		80		%	Average P_{OUT}, 25 °C (230 VAC)
Required average efficiency at 25, 50, 75 and 100 % of P_{OUT}	η_{CEC}	76			%	Per ENERGRY STAR EPS v2
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B				
Safety		Designed to meet IEC950, UL1950 Class II				
Surge						1.2/50 μs surge, IEC 1000-4-5, Series Impedance:
Differential Mode					kV	Differential Mode: 2 Ω
Common Mode					kV	Common Mode: 12 Ω
Ambient Temperature	T_{AMB}	0		50	°C	External case ambient, free convection, sea level

3 Schematic

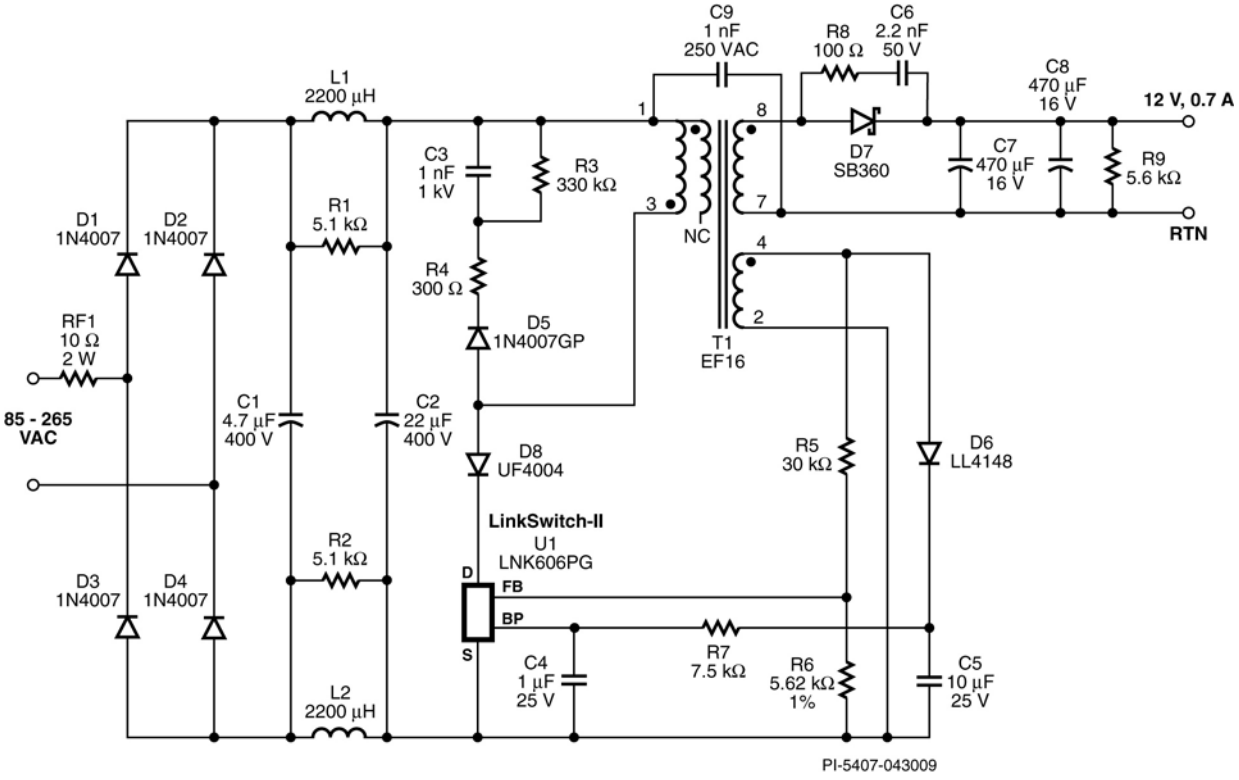

Figure 1 – LED Driver Circuit Schematic.

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4 Circuit Description

This circuit is configured as a primary-side regulated flyback power supply utilizing the LNK606PG.

4.1 Input Filter

AC input power is rectified by diodes D1 through D4. The rectified DC is filtered by the bulk storage capacitors C1 and C2. Components L1, L2, C1 and C2 form a pi (π) filter, which attenuates conducted differential-mode EMI noise. Resistors R1 and R2 damp any ringing between L1 (L2) and C1 (C2) and improve EMI.

4.2 LNK 606 Primary

The LNK606 device (U1) incorporates the power switching device, oscillator, CC/CV control engine, startup, and protection functions. The integrated 700 V MOSFET allows for sufficient voltage margin in universal input AC applications. The device is powered from the BP pin via the decoupling capacitor C4.

The rectified and filtered input voltage is applied to one end of the primary winding of T1. The other side of the transformer's primary winding is driven by the integrated MOSFET in U1. The leakage inductance drain voltage spike is limited by an RCD-R clamp consisting of D5, R3, R4, and C3.

D5 is used to protect the IC from negative ringing (drain voltage below source voltage) when the MOSFET is off, due to the high value of the transformer's VOR.

4.3 Output Rectification

The secondary of the transformer is rectified by D7, a Schottky barrier type for higher efficiency, and filtered by C7 and C8. In this application, Resistor R8 and C6 damp high frequency ringing and improve conducted and radiated EMI.

4.4 Output Regulation

The LNK606 regulates the output using On/Off control in the constant voltage (CV) regulation region of the output characteristic and frequency control for constant current (CC) regulation. The output voltage is sensed by a bias winding on the transformer. The feedback resistors (R5 and R6) were selected using standard 1% resistor values to center both the nominal output voltage and constant current regulation thresholds. The feedback resistors need to be tuned if the same design is used with and without a bias winding.

Resistor R9 provides a minimum load to maintain output regulation. This resistor is only for a self biased design. If the bias winding supply (D6, C5 and R7) is used no pre-load resistor is needed as the energy is absorbed by the bias winding.

5 PCB Layout

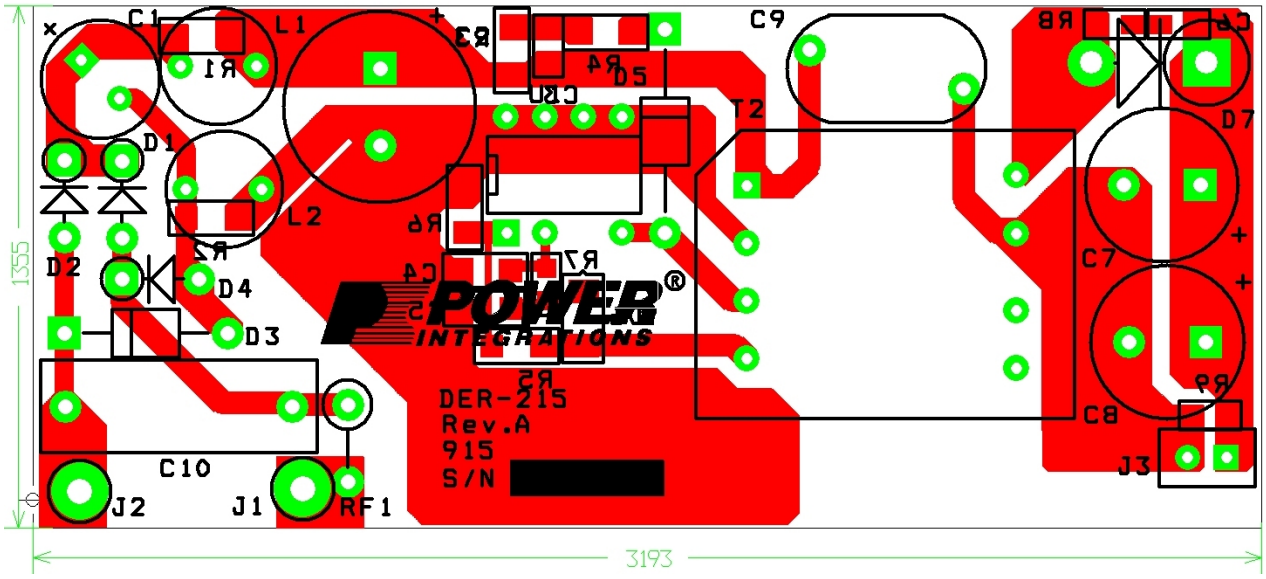

Figure 2 – Printed Circuit Layout.

Note: A location for a 0.1 μF x-capacitor is shown on the PCB. This was not populated during testing nor is required to provide the EMI results shown.

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6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	C1	4.7 μF, 400 V, Electrolytic, (8 x 11.5)	TAQ2G4R7MK0811MLL3	Taicon Corporation
2	1	C2	22 μF, 400 V, Electrolytic, (12.5 x 18)	Not Provided	Samxon
3	1	C3	1 nF, 1000 V, Ceramic, X7R, 0805	C0805C102KDRACTU	Kemet
4	1	C4	1 μF, 25 V, Ceramic, X7R, 1206	ECJ-3YB1E105K	Panasonic
5	1	C5	10 μF, 25 V, Ceramic, X7R, 1206	ECJ-3YB1E106M	Panasonic
6	1	C6	2.2 nF, 50 V, Ceramic, X7R, 0805	ECJ-2VB1H222K	Panasonic
7	2	C7 C8	470 μF, 16 V, Electrolytic, Low ESR, 90 mΩ, (10 x 12.5)	ELXZ160ELL471MJC5S	Nippon Chemi-Con
8	1	C9	1 nF, Ceramic, Y1	ECK-DNA102MB	Panasonic
10	5	D1 D2 D3 D4 D5	1000 V, 1 A, Rectifier, DO-41	1N4007-E3/54	Vishay
11	1	D6	75 V, 0.15 A, Fast Switching, 4 ns, MELF	LL4148-13	Diode Inc.
12	1	D7	60 V, 3 A, Schottky, DO-201AD	SB360	Vishay
13	1	D8	400 V, 1 A, Ultrafast Recovery, 50 ns, DO-41	UF4004-E3	Vishay
14	2	L1 L2	2200 μH, 0.21 A	SBC4-222-211	Tokin
15	2	R1 R2	5.1 kΩ, 5%, 1/4 W, Metal Film, 1206	ERJ-8GEYJ512V	Panasonic
16	1	R3	330 kΩ, 5%, 1/4 W, Metal Film, 1206	ERJ-8GEYJ334V	Panasonic
17	1	R4	300 Ω, 5%, 1/4 W, Metal Film, 1206	ERJ-8GEYJ301V	Panasonic
18	1	R5	30 kΩ, 5%, 1/8 W, Metal Film, 0805	ERJ-6GEYJ303V	Panasonic
19	1	R6	5.62 kΩ, 1%, 1/4 W, Metal Film, 1206	ERJ-8ENF5621V	Panasonic
20	1	R7	7.5 kΩ, 5%, 1/8 W, Metal Film, 0805	ERJ-6GEYJ752V	Panasonic
21	1	R8	100 Ω, 5%, 1/8 W, Metal Film, 0805	ERJ-6GEYJ101V	Panasonic
22	1	R9	5.6 kΩ, 5%, 1/8 W, Metal Film, 0805	ERJ-6GEYJ562V	Panasonic
23	1	RF1	10 Ω, 2 W, Fusible/Flame Proof Wire Wound	CRF253-4 10R	Vitrohm
24	1	T1	Bobbin, EF16, Horizontal, 8 pin, extended creepage	SP 1738 K	Kaschke
25	1	U1	LinkSwitch-II, LNK606PG, CV/CC, DIP-8C	LNK606PG	Power Integrations

7 Transformer Specification

7.1 Electrical Diagram

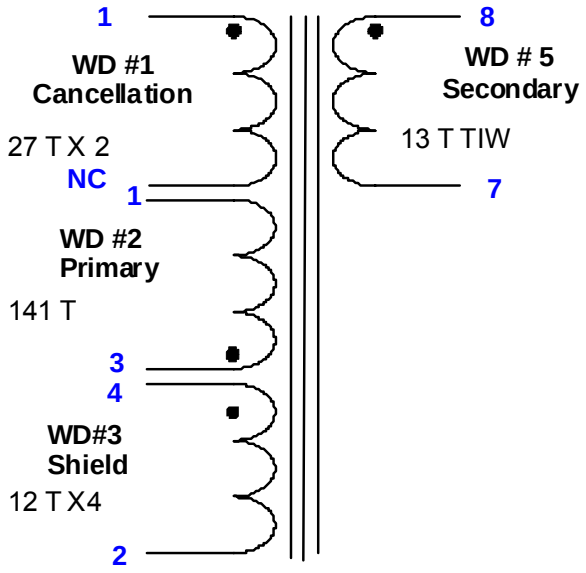

Figure 3 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Electrical Strength	60 second, 60Hz, from pins 1-5 to pins 6-10	3000 VAC
Primary Inductance	Pins 1-3, all other windings open, measured at 100 kHz, 0.4 VRMS	1.714 mH, ±10%
Resonant Frequency	Pins 1-3, all other winding open	500 kHz (min)
Primary Leakage Inductance	Pins 1-3, with pins 7-8 shorted, measured at 100 kHz, 0.4 VRMS	70 μH (max)

7.3 Materials

Item	Description
[1]	Core: PC44, gapped for AL of 86 nH/t2
[2]	Bobbin: Horizontal 8 pin, EF16, extended creepage
[3]	Magnet Wire: 0.15 mm diameter
[4]	Magnet Wire: 0.20 mm diameter
[5]	Triple Insulated Wire: 0.45mm diameter
[6]	Tape, 3M
[7]	Varnish

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7.4 Transformer Build Diagram

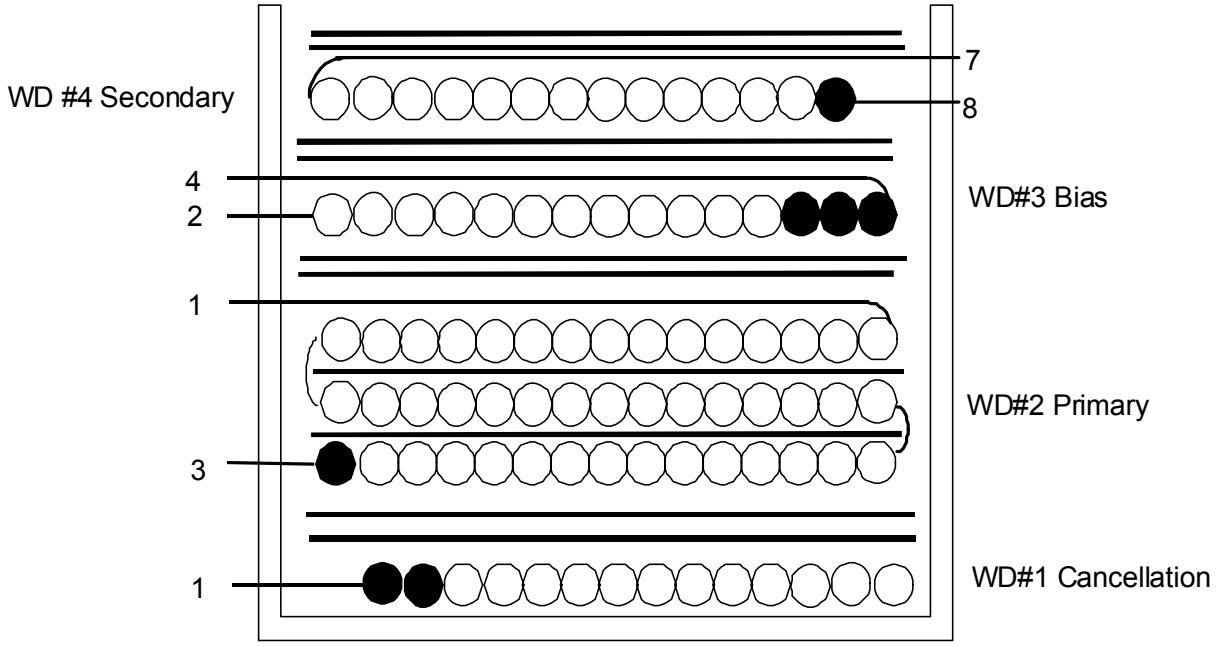

Figure 4 – Transformer Build Diagram.

7.5 Transformer Construction

Bobbin Preparation	Primary side of the bobbin is placed on the left hand side, and secondary side of the bobbin is placed on the right hand side.
WD1 Shield	Primary pin side of the bobbin oriented to left hand side. Start at pin 1. Wind 27 bifilar turns of item [3] from left to right. Wind with tight tension across bobbin evenly. Cut at the end.
Insulation	2 Layers of tape [6] for insulation.
WD2 Primary	Start at Pin 3. Wind 54 turns of item [3] from left to right. Apply one layer of tape [6]. Then wind another 54 turns on the next layer from right to left. Apply one layer of tape [6]. Wind the last 33 turns from left to right. Terminate on pin 1. Wind with tight tension and spread turns across bobbin evenly.
Insulation	2 layers of tape [6] for basic insulation.
WD3 Bias	Starting at pin 5 temporarily, wind 12 trifilar turns of item [4]. Wind from right to left with tight tension spreading turns across entire bobbin width. Finish on pin 2. Flip the starting lead to pin 4.
Insulation	2 layers of tape [6] for basic insulation.
WD4 Secondary	Start at pin 8 wind 13 turns of item [5] from right to left. Spread turns evenly across bobbin. Finish on pin 7.
Insulation	2 layers of tape item [6].
Finish	Grind the core to get 1.714mH. Secure the core with tape. Vanish [7].

Note: Tape between adjacent primary winding layers reduces primary capacitance and losses.

8 Transformer Design Spreadsheet

ACDC_LinkSwitch-II_040908; Rev.1.1; Copyright Power Integrations 2008	INPUT	INFO	OUTPUT	UNIT	ACDC_LinkSwitch-II_040908_Rev1-0.xls; LinkSwitch-II Discontinuous Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					
VACMIN	85			V	Minimum AC Input Voltage
VACMAX	265			V	Maximum AC Input Voltage
fL	50			Hz	AC Mains Frequency
VO	12			V	Output Voltage (at continuous power)
IO	0.7			A	Power Supply Output Current (corresponding to peak power)
Power		*Warning*	8.40	W	!!! Warning. Continuous Output power is too high. Use larger LinkSwitch-II device
n	0.76		0.76		Efficiency Estimate at output terminals. Under 0.7 if no better data available
Z			0.50		Z Factor. Ratio of secondary side losses to the total losses in the power supply. Use 0.5 if no better data available
tC			3.00	ms	Bridge Rectifier Conduction Time Estimate
Add Bias Winding			NO		Choose Yes to add a Bias winding to power the LinkSwitch-II.
CIN	26.7			uF	Input Capacitance
ENTER LinkSwitch-II VARIABLES					
Chosen Device	**LNK606**		LNK606		Chosen LinkSwitch-II device
Package	**PG**		PG		Select package (PG, GG or DG)
ILIMITMIN			0.39	A	Minimum Current Limit
ILIMITTYP			0.41	A	Typical Current Limit
ILIMITMAX			0.45	A	Maximum Current Limit
FS	67.5		67.50	kHz	Typical Device Switching Frequency at maximum power
VOR		*Warning*	135.58	V	!!! Warning. Reflected Output Voltage too high. Increase DCON or Increase FSMAX
VDS	3		3.00	V	LinkSwitch-II on-state Drain to Source Voltage
VD			0.50	V	Output Winding Diode Forward Voltage Drop
KP			1.88		Ensure KDP > 1.3 for discontinuous mode operation
FEEDBACK WINDING PARAMETERS					
NFB			12.00		Feedback winding turns
VFLY			11.54	V	Flyback Voltage
VFOR			7.92	V	Forward voltage
BIAS WINDING PARAMETERS					
VB			N/A	V	Output Voltage is greater than 10 V. The feedback winding itself can be used to provide exteral bias to the LinkSwitch. Additional Bias winding is not required.
NB			N/A		Bias Winding number of turns
DESIGN PARAMETERS					
DCON	4.5		4.50	us	Output diode conduction time
TON			6.46	us	LinkSwitch-II On-time (calculated at minimum inductance)
RUPPER			30.79	k-ohm	Upper resistor in Feedback resistor divider
RLOWER			5.69	k-ohm	Lower resistor in resistor divider
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type					
Core	**EF16**		EF16		Enter Transformer Core. Based on the output power the recommended core sizes are EEL19 or EEL22
Bobbin			EF16_		Generic EF16_BOBBIN

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			BOBBIN		
AE			20.10	mm^2	Core Effective Cross Sectional Area
LE			37.60	mm^2	Core Effective Path Length
AL			1100.00	nH/turn^2	Ungapped Core Effective Inductance
BW			10.00	mm	Bobbin Physical Winding Width
M			0.00	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L	3		3.00		Number of Primary Layers
NS			13.00		Number of Secondary Turns. To adjust Secondary number of turns change DCON
DC INPUT VOLTAGE PARAMETERS					
VMIN			93.03	V	Minimum DC bus voltage
VMAX			374.77	V	Maximum DC bus voltage
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.44		Maximum duty cycle measured at VMIN
IAVG			0.12	A	Input Average current
IP			0.39	A	Peak primary current
IR			0.39	A	Primary ripple current
IRMS			0.17	A	Primary RMS current
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LPMIN			1542.94	uH	Minimum Primary Inductance
LPTYP			1714.38	uH	Typical Primary inductance
LP_TOLERANCE			10.00		Tolerance in primary inductance
NP			141.00		Primary number of turns. To adjust Primary number of turns change BM_TARGET
ALG			86.23	nH/turn^2	Gapped Core Effective Inductance
BM_TARGET	2490		2490.00	Gauss	Target Flux Density
BM			2480.14	Gauss	Maximum Operating Flux Density (calculated at nominal inductance), BM < 2500 is recommended
BP		*Warning*	3000.97	Gauss	!!! Warning. Peak Flux density exceeds 3000 Gauss and is not recommended. Reduce BP by increasing NS
BAC			1240.07	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			163.75		Relative Permeability of Ungapped Core
LG			0.30	mm	Gap Length (LG > 0.1 mm)
BWE			30.00	mm	Effective Bobbin Width
OD			0.21	mm	Maximum Primary Wire Diameter including insulation
INS			0.04		Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.17	mm	Bare conductor diameter
AWG			34.00		Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			40.32		Bare conductor effective area in circular mils
CMA			234.48		Primary Winding Current Capacity (200 < CMA < 500)
TRANSFORMER SECONDARY DESIGN PARAMETERS					
Lumped parameters					
ISP			4.22	A	Peak Secondary Current
ISRMS			1.54	A	Secondary RMS Current
IRIPPLE			1.38	A	Output Capacitor RMS Ripple Current
CMS			308.96		Secondary Bare Conductor minimum circular mils
AWGS			25.00		Secondary Wire Gauge (Rounded up to next larger standard AWG value)
VOLTAGE STRESS PARAMETERS					
VDRAIN			679.48	V	Maximum Drain Voltage Estimate (Assumes 20% clamping voltage tolerance and an additional 10% temperature tolerance)

PIVS			46.55	V	Output Rectifier Maximum Peak Inverse Voltage
FINE TUNING					
RUPPER_ACTUAL	30			k-ohm	Actual Value of upper resistor (RUPPER) used on PCB
RLOWER_ACTUAL	5,6			k-ohm	Actual Value of lower resistor (RLOWER) used on PCB
Actual (Measured) Output Voltage (VDC)				V	Measured Output voltage from first prototype
Actual (Measured) Output Current (ADC)				Amps	Measured Output current from first prototype
RUPPER_FINE			30.00	k-ohm	New value of Upper resistor (RUPPER) in Feedback resistor divider. Nearest standard value is 30,1 k-ohms
RLOWER_FINE			5.60	k-ohm	New value of Lower resistor (RLOWER) in Feedback resistor divider. Nearest standard value is 5,62 k-ohms

Note: Spreadsheet values may be different from values generated from different spreadsheet revisions.

The spreadsheet flags 3 warnings:

1) PO – The data sheet figures for maximum output power is 6 W. This power was recommended for a 5 V output. As this design is for a 12 V output and the thermal performance is acceptable, this warning can be ignored.
2) VOR – This warning appears if VOR > 135 V. As in this design, the peak drain voltage VDRAIN < 680 V, this warning can be ignored.
3) BP – This warning shows up if BP > 3000 Gauss. In this design, this guideline is only slightly violated. Since no transformer saturation was seen, this warning can be ignored.

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9 Performance Data

All measurements performed at room temperature unless otherwise specified, 50 Hz input frequency.

9.1 Efficiency

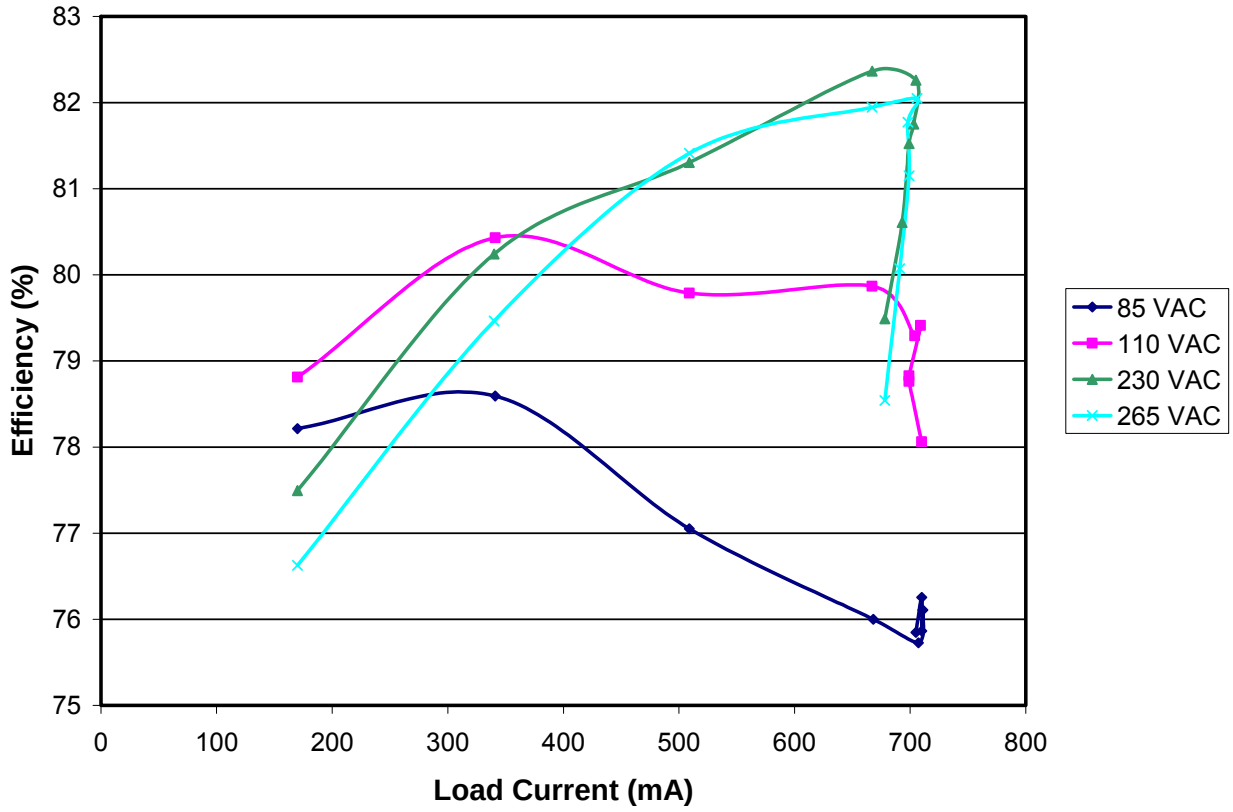

Figure 5 – Efficiency vs. Output Power.

9.2 Active Mode Efficiency

Percent of Full Load	Efficiency (%)	
	115 VAC	230 VAC
25	78.8	77.5
50	80.4	80.3
75	79.8	81.3
100	79.3	81.6
Average	**79.6**	**80.1**
US EISA (2007) requirement	79.5	
ENERGY STAR 2.0 requirement	79.5	

Figure 6 – Efficiency vs. Input Voltage and Load, Room Temperature, 50 Hz.

9.3 Energy Efficiency Requirements

The external power supply requirements below all require meeting active mode efficiency and no-load input power limits. Minimum active mode efficiency is defined as the average efficiency of 25, 50, 75 and 100% of output current (based on the nameplate output current rating).

For adapters that are single input voltage only then the measurement is made at the rated single nominal input voltage (115 VAC or 230 VAC), for universal input adapters the measurement is made at both nominal input voltages (115 VAC and 230 VAC).

To meet the standard the measured average efficiency (or efficiencies for universal input supplies) must be greater than or equal to the efficiency specified by the standard.

The test method can be found here:

http://www.energystar.gov/ia/partners/prod_development/downloads/power_supplies/EPSupplyEffic_TestMethod_0804.pdf

For the latest up to date information please visit the PI Green Room:

http://www.powerint.com/greenroom/regulations.htm

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9.3.1 USA Energy Independence and Security Act 2007

This legislation mandates all single output single output adapters, including those provided with products, manufactured on or after July 1st, 2008 must meet minimum active mode efficiency and no load input power limits.

Active Mode Efficiency Standard Models

Nameplate Output (P_O)	Minimum Efficiency in Active Mode of Operation
< 1 W	$0.5 \times P_O$
≥ 1 W to ≤ 51 W	$0.09 \times \ln(P_O) + 0.5$
> 51 W	0.85

ln = natural logarithm

No-load Energy Consumption

Nameplate Output (P_O)	Maximum Power for No-load AC-DC EPS
All	≤ 0.5 W

This requirement supersedes the legislation from individual US States (for example CEC in California).

9.3.2 ENERGY STAR EPS Version 2.0

This specification takes effect on November 1st, 2008.

Active Mode Efficiency Standard Models

Nameplate Output (P_O)	Minimum Efficiency in Active Mode of Operation
≤ 1 W	$0.48 \times P_O + 0.14$
> 1 W to ≤ 49 W	$0.0626 \times \ln(P_O) + 0.622$
> 49 W	0.87

ln = natural logarithm

Active Mode Efficiency Low Voltage Models (V_O<6 V and $I_O \geq 550$ mA)

Nameplate Output (P_O)	Minimum Efficiency in Active Mode of Operation
≤ 1 W	$0.497 \times P_O + 0.067$
> 1 W to ≤ 49 W	$0.075 \times \ln(P_O) + 0.561$
> 49 W	0.86

ln = natural logarithm

No-load Energy Consumption (both models)

Nameplate Output (P_O)	Maximum Power for No-load AC-DC EPS
0 to < 50 W	≤ 0.3 W
≥ 50 W to ≤ 250 W	≤ 0.5 W

9.4 No-Load Input Power

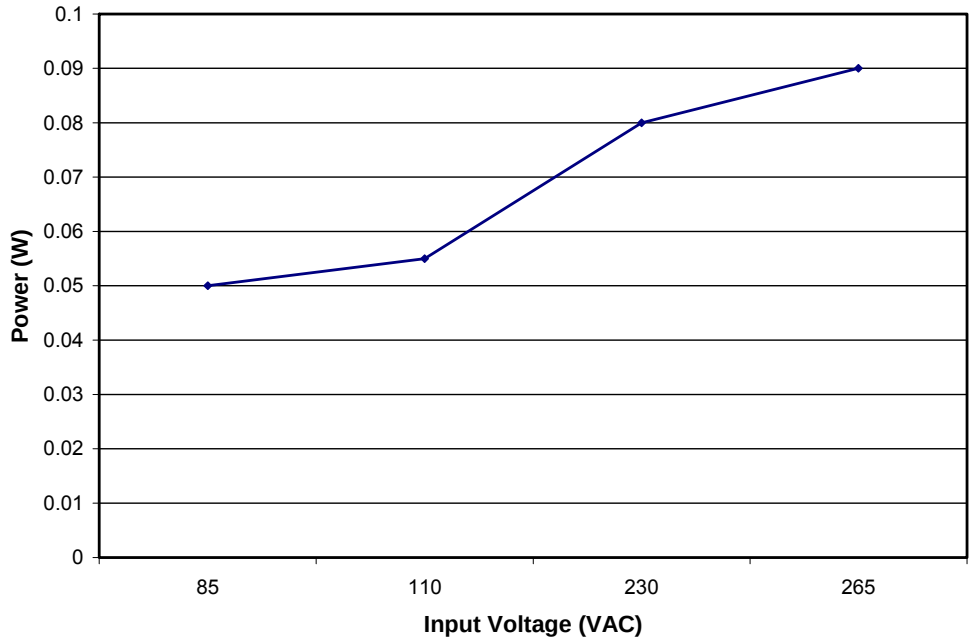

Figure 7 – Zero Load Input Power vs. Input Line Voltage, Room Temperature, 50 Hz.

9.5 Regulation

9.5.1 Load

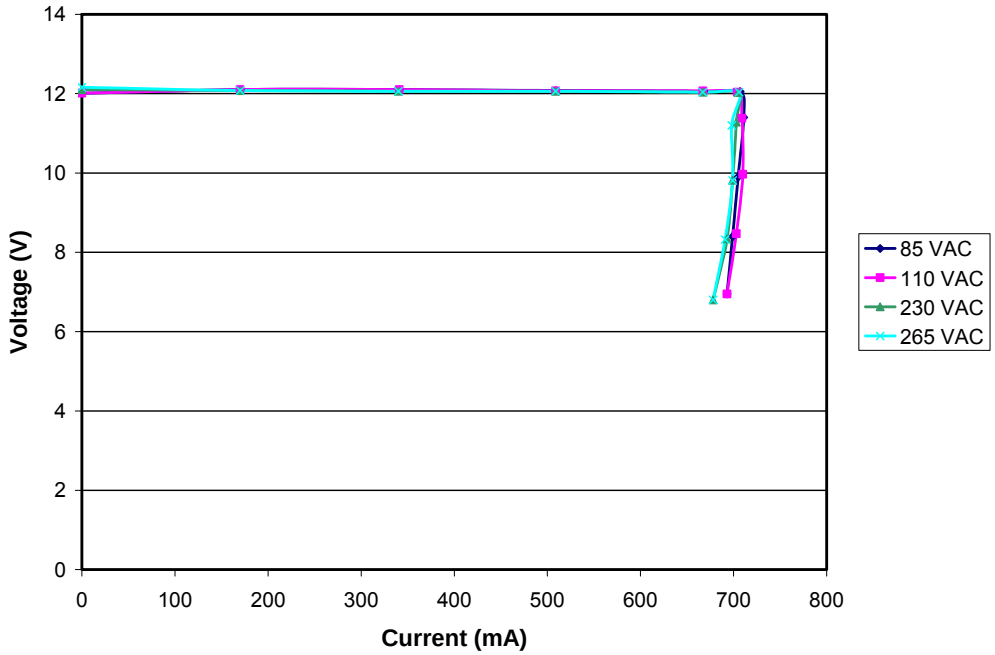

Figure 8 – Typical CC/CV Characteristic at Ambient Temperature.

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10 Thermal Performance

Measurements made at full load, 50Hz electric system.

Item	115 VAC	230 VAC
Ambient	25 ^{0}C	25 ^{0}C
LNK606PG (U1)	52 ^{0}C	56 ^{0}C
T1 Transformer	49 ^{0}C	50 ^{0}C

11 Waveforms

11.1 Drain Voltage and Current, Normal Operation

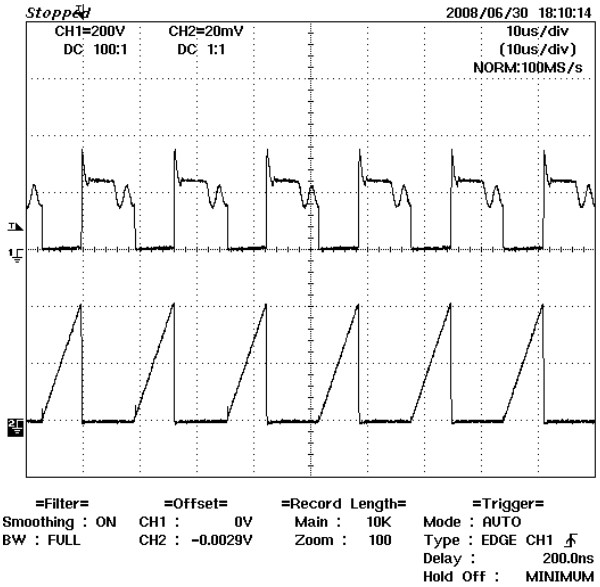

Figure 9 – 85 VAC, Full Load.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 200 mA / div, 10 μs / div.

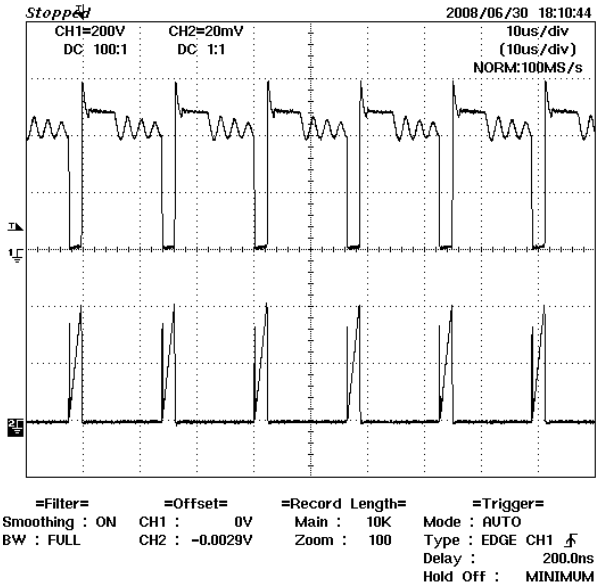

Figure 10 – 265 VAC, Full Load.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 200 mA / div, 10 us / div.

11.2 Output Voltage Start-up Profile

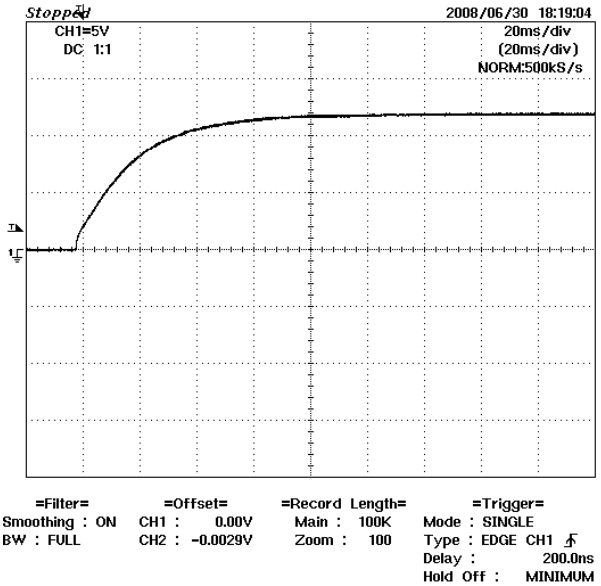

Figure 11 – Start-up Profile (Full load), 85 VAC
5 V, 20 ms / div.

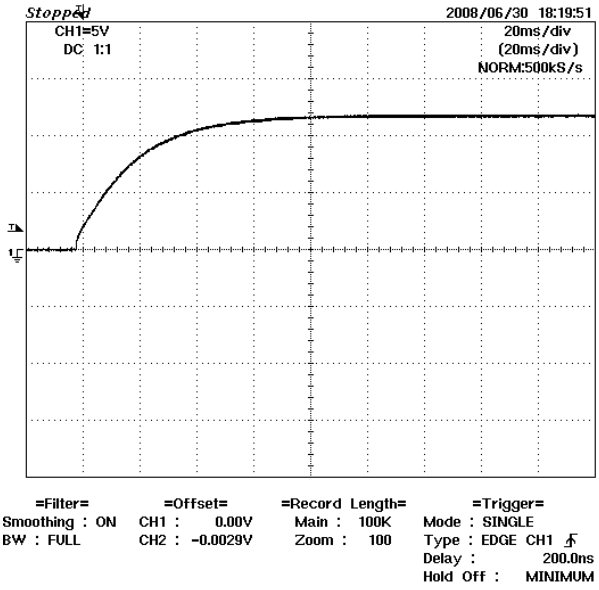

Figure 12 – Start-up Profile (Full Load), 265 VAC
5 V, 20 ms / div.

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11.3 Drain Voltage and Current Start-up Profile

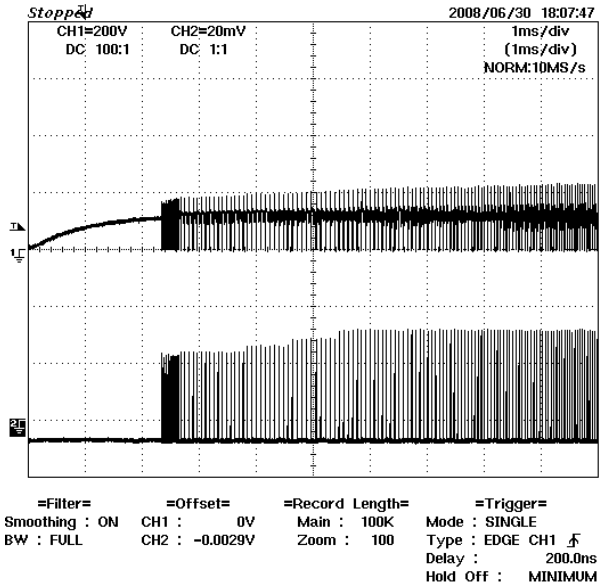

Figure 13 – 85 VAC Input and Maximum Load.
Upper: V_{DRAIN}, 200 V & 1 ms / div.
Lower: I_{DRAIN}, 200 mA / div.

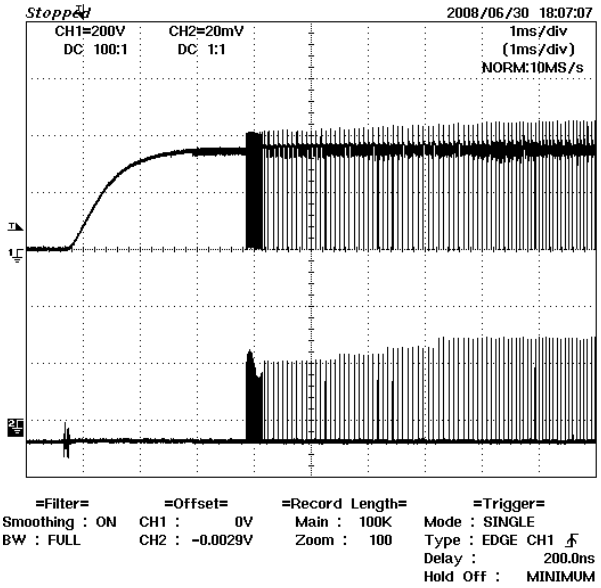

Figure 14 – 265 VAC Input and Maximum Load.
Upper: V_{DRAIN}, 200 V & 1 ms / div.
Lower: I_{DRAIN}, 200 mA / div.

11.4 Output Ripple Measurements

11.4.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pickup. Details of the probe modification are provided below.

The 5125BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 10 μF/50 V aluminum electrolytic. ***The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).***

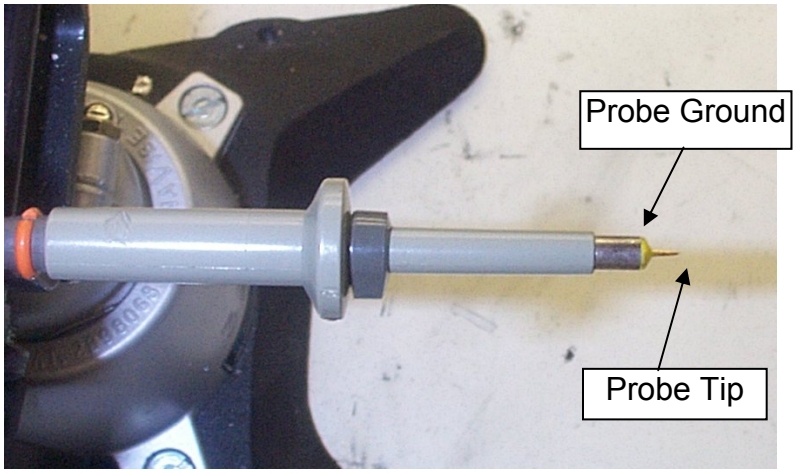

Figure 15 – Oscilloscope Probe Prepared for Ripple Measurement (End Cap and Ground Lead Removed).

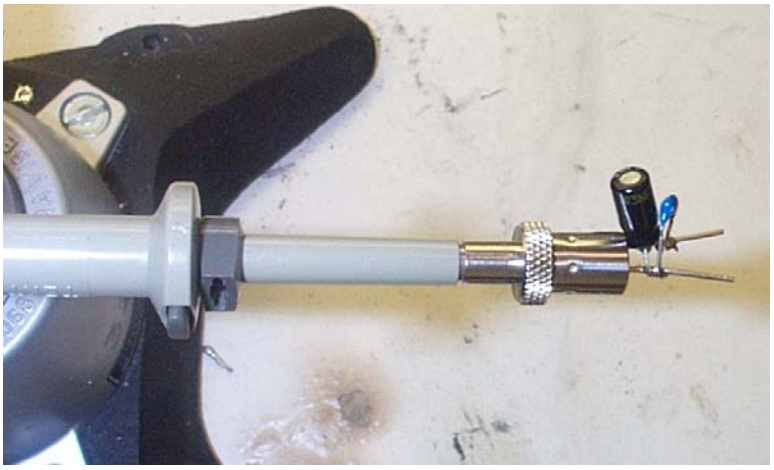

Figure 16 – Oscilloscope Probe with Probe Master 5125BA BNC Adapter (Modified with Wires for Probe Ground for Ripple measurement and Two Parallel Decoupling Capacitors Added).

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11.4.2 Measurement Results

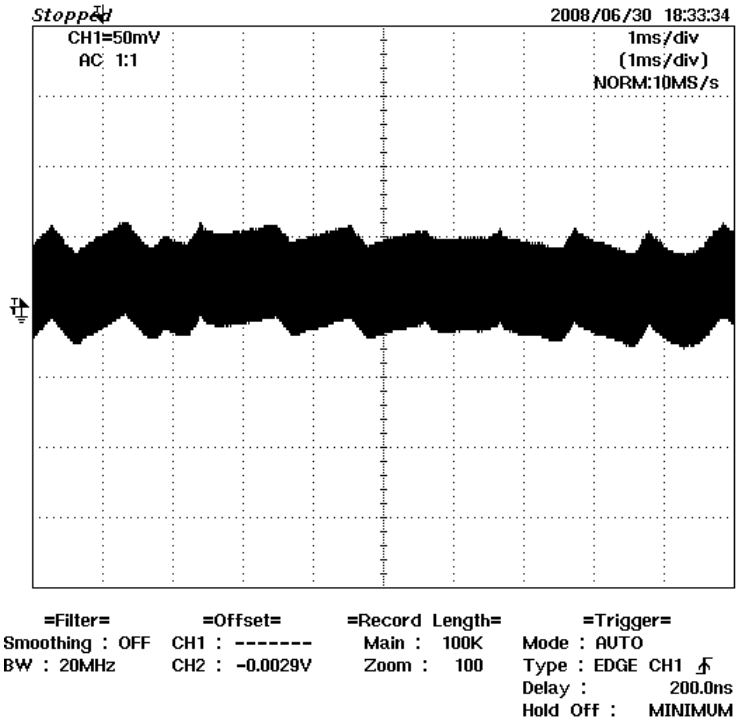

Figure 17 – Ripple, 85 VAC, Full Load, 50 mV, 1 ms / div.

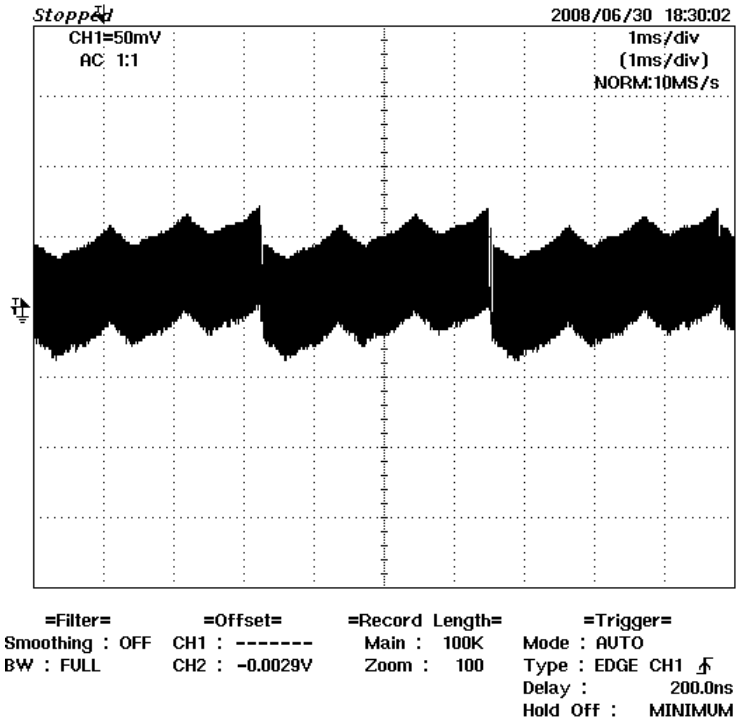

Figure 18 – Ripple, 265 VAC, Full Load, 50 mV, 1 ms / div.

12 Conducted EMI

All Conducted EMI tests were made using the artificial hand connected to the secondary return.

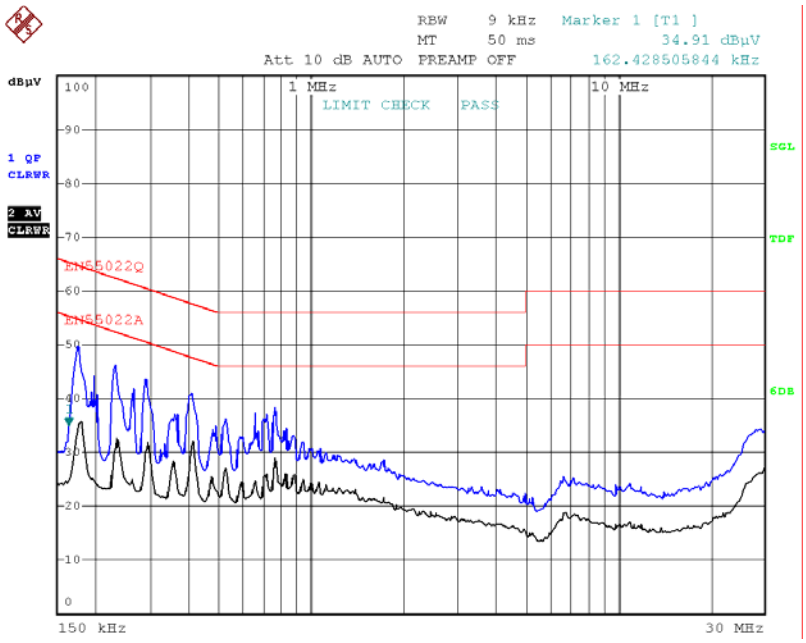

Figure 19 – Conducted EMI, 115 VAC, Line, Full load, EN55022Q: QP Limit; EN55022A: Average Limit; Blue: QP Scan; Black: Average Scan.

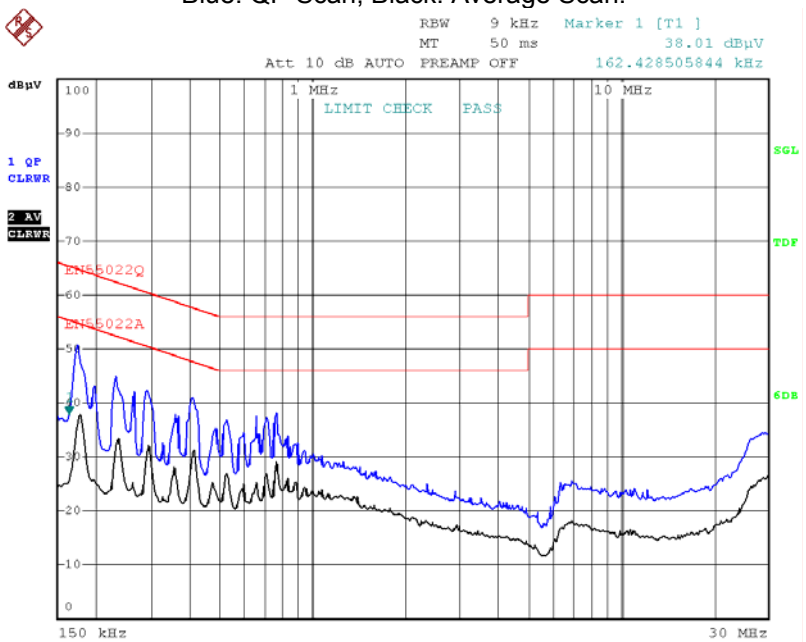

Figure 20 – Conducted EMI, 115 VAC, Neutral, Full Load, EN55022Q: QP Limit; EN55022A: Average Limit; Blue: QP Scan; Black: Average Scan.

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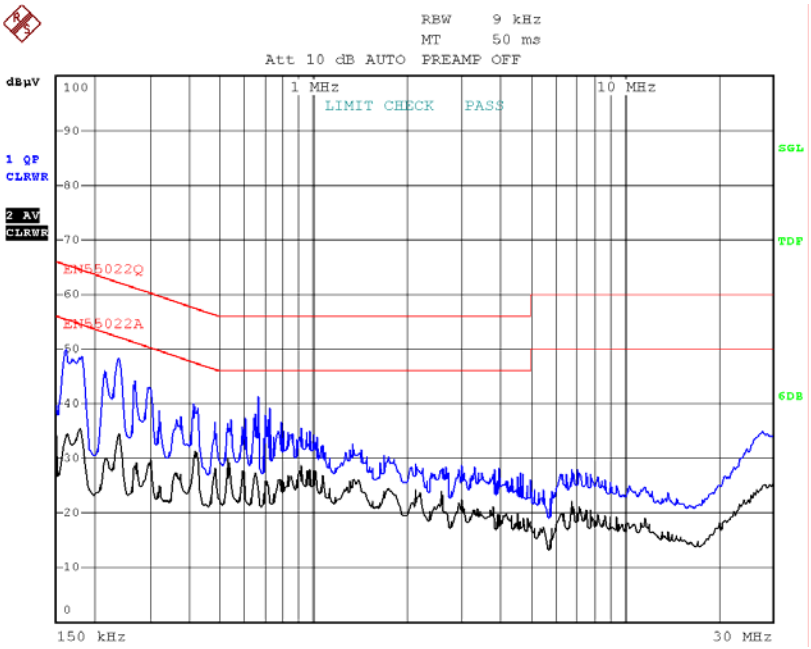

Figure 21 – Conducted EMI, 230 VAC, Line, Full Load, EN55022Q: QP limit; EN55022A: Average Limit; Blue: QP Scan; Black: Average Scan.

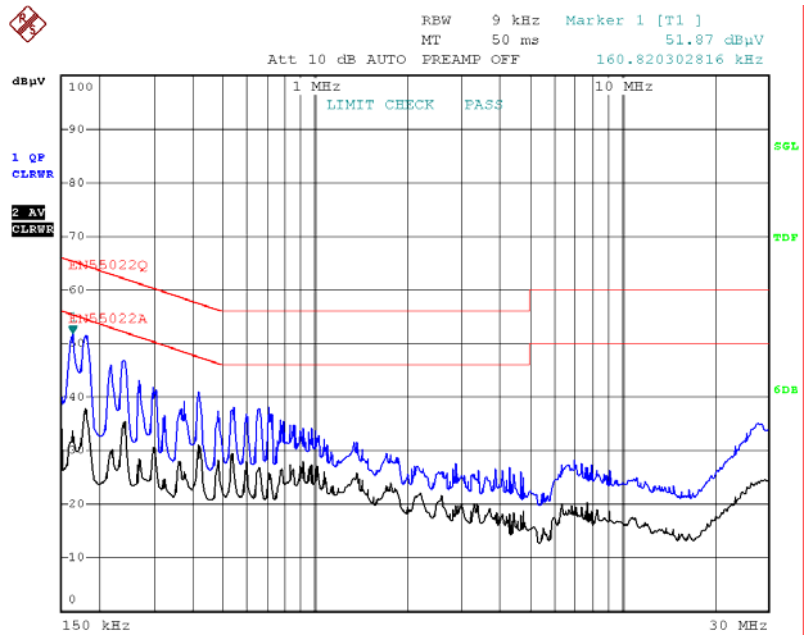

Figure 22 – Conducted EMI, 230 VAC, Neutral, Full load, EN55022Q: QP Limit; EN55022A: Average Limit; Blue: QP Scan; Black: Average Scan.

13 Revision History

Date	Author	Revision	Description & changes	Reviewed
01-May-09	RP	1.0	Initial Release	Apps & Mktg

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